AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 12, line 10, with the following rewritten paragraph:

Once the SRAM cache 34 mounted on the ceramic substrate 32 is tested and deemed satisfactory, the combined cache 34 and ~~side of the substrate 32 that does not have the SRAM 34 cache mounted to it~~ substrate 32 is attached to a shelf 18 of ceramic package 17, with the ceramic substrate 32 functioning as a lid above the CPU die 26 (step 62). Note that substrate 32 can have a metallized surface for traces, or can utilize a multi-layer ceramic approach. Regardless, the substrate 32 can function both as a lid for the multi-chip package 10 as well as a component for carrying a device such as the SRAM cache 34. A seal 42 is between the base of the substrate 32 and the upper edge of the shelf 18 it resides on. In one embodiment, the seal 42 is an eutetic seal; the seal 42 may also be an epoxy. In this manner, an open cavity 44 with no filler protects the CPU die 26. The seal 42 provides an environmental seal in addition to providing structural support between substrate 32 and package 17.--

Please replace the paragraph beginning at page 14, line 1, with the following rewritten paragraph:

--Once the SRAM cache 74 mounted on the ceramic substrate 32 is tested and deemed satisfactory, the combined cache 74 and substrate 32 ~~side of the substrate 32 that does not have the SRAM cache 74 mounted to it~~ is attached to a shelf 18 of ceramic package 17, with the ceramic substrate 32 functioning as a lid above the CPU die 26 (step 62). A seal 42 is between the base of the substrate

32 and the upper edge of the shelf 18 it resides on. In this manner, an open cavity 44, with no filler protects the CPU die 26. After the substrate 32 has been attached and sealed to the shelf 18 of the ceramic package 17, the substrate 32 is electrically connected to the ceramic pakage 17 using wire bond II 38 (step 64). In this manner, the SRAM cache 74 is electrically coupled to the chip package 17. The multi-chip package 70 is then filled (above the SRAM cache 34 and substrate 32) with an encapsulant 40 (step 66). Once the multi-chip package 70 is fully fabricated, a final functionality test may be applied to the device as a whole (step 68).--

Please replace the paragraph beginning at page 15, line 14, with the following rewritten paragraph:

--Once the SRAM cache 74 mounted on the organic substrate 91 is tested and deemed satisfactory, the combined cache 74 and substrate 91 ~~side of the substrate 91 that does not have the SRAM cache 74 mounted to it~~ is attached to a shelf 18 of organic package 93, with the organic substrate 91 functioning as a lid above the CPU die 26 (step 110). A seal 42 is between the base of the substrate 91 and the upper edge of the shelf 18 it resides on. After the substrate 91 has been attached and sealed to the shelf 18 of the organic packago the organic package 93 using wire bonds II 38 (112). In this manner, the SRAM cache 74 is electrically coupled to the chip package 93. The multi-chip package 90 is filled (above the SRAM cache 74 and substrate 91) with a second encapsulant 40 (step 114). Once the multi-chip package 90 is fully fabricated, a final functionality test may be applied to the device as a whole (step 116).--

Please replace the paragraph beginning at page 16, line 20, with the following rewritten paragraph:

Once the SRAM cache 132 mounted on the ceramic substrate 128 is tested and deemed satisfactory, the combined cache 132 and substrate 128 ~~side of the substrate 128 that does not have the SRAM cache 132 mounted to it~~ is attached to a shelf 16 of organic package 93, with the ceramic substrate 128 functioning as a lid above the semiconductor die 124. After the substrate 128 has been attached and sealed to the shelf 16 of the organic package 93, the substrate 128 is electrically connected to the organic package 93 using wire bond III 136. In this manner, the SRAM cache 132 is electrically coupled to the chip package 93. The multi-chip package 118 is filled (above the SRAM cache 132 and substrate 128) with an encapsulant 138. The partially fabricated multi-chip package 118 may be tested for functionality at this stage of fabrication also before proceeding.